REMARKS

This responds to the Office Action mailed on February 7, 2005.

Claims 1, 10, 16, 20, 24, 29, and 34 are amended, claims 8 and 9 are canceled, and no claims are added; as a result, claims 1-6, 10-14, 16-18, 20-22, 24-27, 29-32, and 34-37 are now pending in this application.

Replacement Drawing Sheet

Applicant submitted a Replacement Drawing Sheet 7 with the response filed on January 5, 2005. The replacement sheet included the identifier for Fig. 2H, which had been omitted. Applicant respectfully requests the explicit approval of this correction.

§103 Rejection of the Claims

Claims 1-5, 20, 21, and 24-26 were rejected under 35 USC § 103(a) as being unpatentable over Gardner et al. (U.S. 6,268,637) in view of Delgado et al. (U.S. 5,949,144). Claims 6, 8, 9, 22, 27, 32, and 37 were rejected under 35 USC § 103(a) as being unpatentable over Gardner et al. in view of Delgado et al. as applied to claims 1, 20, and 24, and further in view of Schwank et al. (U.S. 6,268,630). Applicant does not admit that Gardner is indeed prior art and reserves the right to swear behind this reference at a later date. Applicant respectfully traverses the 35 USC § 103(a) rejection for at least the following reasons.

The rejection of claim 9 on page 4 states that under a combination with the Schwank reference, "the trench will extend at least partially into a level of the dielectric layer of the substrate."

Gardner appears to show a pair of devices 18, 20 formed in active areas 22 and 24 of a substrate 12. Gardner also appears to show an air gap 62 in a trench 58. Gardner does not show a dielectric layer with an air gap for location at least partially beneath an active region and a semiconductor layer formed over the dielectric layer. Gardner does not show any dielectric layer within a substrate. Gardner also does not show a trench that extends at least partially into a level of a dielectric layer.

Delgado appears to show a trench 40. The trench in Delgado is formed "by etching device wafer 14 and stopping the etch on the oxide layer 22." Delgado does not show a trench that extends at least partially into a level of a dielectric layer.

Schwank appears to show an SOI wafer 16 and field oxide 30 located in trenches 26 that are formed up to a buried oxide layer 20. However, Schwank does not show a trench that extends at least partially into a level of a dielectric layer.

Applicant respectfully submits that Gardner cannot teach a depth into a dielectric layer, because as stated above, Gardner does not show any dielectric layer within a substrate. Any assumptions about where a dielectric layer would be located if references were combined is mere speculation. As discussed above, the configurations actually shown in the references do not show a trench that extends at least partially into a level of a dielectric layer.

In contrast, claims 1 and 20 as amended include a trench that extends at least partially into a level of the dielectric layer of the substrate. Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 1 and 20. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Regarding independent claim 24, Delgado also appears to show a cavity 30 formed on a surface of a handle wafer 16. The handle wafer is later bonded to a device wafer 14. Delgado does not show a dielectric layer as claimed *formed within a portion of a semiconductor layer.* The air gap in Delgado is formed separately from the semiconductor layer, and not formed within a portion of a semiconductor layer. Gardner and Schwank also do not show a dielectric layer formed within a portion of a semiconductor layer, the dielectric layer including an air gap for location at least partially beneath an active region.

In contrast, claim 24 as amended includes a dielectric layer formed within a portion of a semiconductor layer, the dielectric layer including an air gap for location at least partially beneath an active region.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claim 24, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claim 24 and claims that depend therefrom.

Claims 10-14, 16-18, 29-31, and 34-36 were rejected under 35 USC § 103(a) as being unpatentable over Gardner et al., Delgado et al., and further in view of Schwank et al. with additional references of Chiang and Beyer in various combinations. Applicant respectfully submits that the additional references of Chiang and Beyer fail to cure the rejections based on Gardner, Delgado, and Schwank for at least the reasons outlined above.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to claims 10-14, 16-18, 29-31, and 34-36.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31 day of March, 2005.

KACIA LEE

Name

Kacia Lee

Signature